IN THE CLAIMS

The current claims follow. For claims not marked as amended in this response, any difference in the claims below and the previous state of the claims is unintentional and in the nature of a typographical error.

1. (Original) For use in a router, a lookup circuit for translating received addresses into destination addresses comprising:

M pipelined memory circuits for storing a trie table capable of translating a first received address into a first destination address, wherein said M memory circuits are pipelined such that a first portion of said first received address accesses an address table in a first memory circuit and an output of said first memory circuit accesses an address table in a second memory circuit.

2. (Original) The lookup circuit as set forth in Claim 1, wherein said output of said first memory circuit comprises a first address pointer that indexes a start of said address table in said second memory circuit.

3. (Original) The lookup circuit as set forth in Claim 2, wherein said first address pointer and a second portion of said first received address access said address table in said second memory circuit.

4. (Original) The lookup circuit as set forth in Claim 3, wherein an output of said second memory circuit accesses an address table in a third memory circuit.

5. (Original) The lookup circuit as set forth in Claim 4, wherein said output of said second memory circuit comprises a second address pointer that indexes a start of said address table in said third memory circuit.

6. (Original) The lookup circuit as set forth in Claim 5, wherein said second address pointer and a third portion of said first received address access said address table in said third memory circuit.

7. (Original) The lookup circuit as set forth in Claim 6, wherein address pointers output from said M pipelined memory circuits are selectively applied to a final memory circuit storing a routing table, said routing table comprising a plurality of destination addresses associated with said received addresses.

8. (Original) The lookup circuit as set forth in Claim 7, further comprising a memory interface capable of selectively applying to said final memory circuit an address pointer associated with said first received address and an address pointer associated with a subsequently received address, such that said address pointer associated with said first received address is applied

to said final memory circuit prior to said address pointer associated with said subsequently received address.

9. (Original) The lookup circuit as set forth in Claim 8, wherein said M pipelined memory circuits comprise static random access memory (SRAM) circuits.

10. (Original) The lookup circuit as set forth in Claim 9, wherein said final memory circuit comprises a dynamic random access memory (DRAM) circuit.

11. (Original) A router for interconnecting N interfacing peripheral devices, said router comprising:

a switch fabric; and

a plurality of routing nodes coupled to said switch fabric, each of said routing nodes comprising:

a plurality of physical medium device (PMD) modules capable of transmitting data packets to and receiving data packets from selected ones of said N interfacing peripheral devices;

an input-output processing (IOP) module coupled to said PMD modules and said switch fabric and capable of routing said data packets between said PMD modules and said switch fabric and between said PMD modules; and

a lookup circuit associated with said IOP module for translating received addresses associated with said data packets into destination addresses, said lookup circuit comprising M pipelined memory circuits for storing a trie table capable of translating a first received address into a first destination address, wherein said M memory circuits are pipelined such that a first portion of said first received address accesses an address table in a first memory circuit and an output of said first memory circuit accesses an address table in a second memory circuit.

12. (Original) The router as set forth in Claim 11, wherein said output of said first memory circuit comprises a first address pointer that indexes a start of said address table in said second memory circuit.

13. (Original) The router as set forth in Claim 12, wherein said first address pointer and a second portion of said first received address access said address table in said second memory circuit.

14. (Original) The router as set forth in Claim 13, wherein an output of said second memory circuit accesses an address table in a third memory circuit.

15. (Original) The router as set forth in Claim 14, wherein said output of said second memory circuit comprises a second address pointer that indexes a start of said address table in said third memory circuit.

16. (Original) The router as set forth in Claim 15, wherein said second address pointer and a third portion of said first received address access said address table in said third memory circuit.

17. (Original) The router as set forth in Claim 16, wherein address pointers output from said M pipelined memory circuits are selectively applied to a final memory circuit storing a routing table, said routing table comprising a plurality of destination addresses associated with said received addresses.

18. (Original) The router as set forth in Claim 17, further comprising a memory interface capable of selectively applying to said final memory circuit an address pointer associated with said first received address and an address pointer associated with a subsequently received address, such that said address pointer associated with said first received address is applied to said final memory circuit prior to said address pointer associated with said subsequently received address.

19. (Original) The router as set forth in Claim 18, wherein said M pipelined memory circuits comprise static random access memory (SRAM) circuits.

20. (Original) The router as set forth in Claim 19, wherein said final memory circuit comprises a dynamic random access memory (DRAM) circuit.

21. (Original) A method for translating a first received address into a first destination address using M pipelined memory circuits that store a trie table, the method comprising the steps of:

accessing an address table in a first memory circuit using a first portion of the first received address;

outputting from the address table in the first memory circuit a first address pointer that indexes a start of an address table in a second memory circuit; and

accessing the address table in the second memory circuit using the first address pointer and a second portion of the first received address.

22. (Original) The method as set forth in Claim 21 further comprising the steps of:

outputting from address table in the second memory circuit a second address pointer that indexes a start of an address table in a third memory circuit; and

accessing the address table in the third memory circuit using the second address pointer and a third portion of the first received address.